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DESIGN OF GRID SYNCHRONISATION METHOD UNDER HARMONIC POLLUTION CONDITIONS

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Abstract

Due to the voltage imbalance in the grid, a significant number of harmonic components are present, often resulting in the failure of conventional phase-locked loop (PLL) systems to accurately track the fundamental phase. To address this challenging issue, a dual second-order all-pass filter (DSOAPF) is designed based on the second-order all-pass filter (SOAPF), enabling the accurate extraction of the fundamental positive sequence component (FPSC) from the three-phase power grid. Building upon this, a combined filter, comprising a DSOAPF and a comb filter (CF), is proposed and integrated into the PLL structure. Through Simulink simulations and analysis under voltage imbalance and harmonic conditions, the results demonstrate that this approach outperforms traditional PLL methods in terms of fundamental voltage phase tracking. Furthermore, it effectively extracts both positive and negative sequence amplitudes, thereby enhancing the rapidity, stability, anti-interference capability, and overall effectiveness of grid-connected power systems.

Key Words

Second-order all-pass filter (SOAPF), harmonic, phase-locked loop (PLL), comb filter (CF)

1. Introduction

Recently, the world has witnessed an increasing energy and environmental problem, which has led to significant advancements in renewable energy power generation technologies. One such technology is distributed generation (DG), where renewable energy generation devices are connected to the grid. DG technology enables stable and reliable electricity output [1]–[3]. By utilising inverters and other equipment, DG technology facilitates the seamless integration and operation with the three-phase power grid, offering advantages, such as flexibility, cost-effectiveness, and environmental friendliness. Grid synchronisation refers to the synchronisation of DG's output voltage with the power grid. Specifically, both voltages operate at the same frequency and phase, forming the foundation for establishing a connection between DG and the power grid [4]–[6]. Common grid synchronisation technologies include voltage zero crossing detection [7], Kalman filter, discrete Fourier transform, and phase-locked loop (PLL). Among them, PLL, as the most widely used grid synchronisation technology in the field of electrical engineering, is an essential and important equipment in distributed power grid connection. The PLL not only detects the grid voltage useful information but also performs anti-disturbance functions. The behaviour of the PLL directly impacts the overall performance of the distributed control system [8]–[10].

Currently, power electronic technology is undergoing rapid development, and its significance in the power grid is increasing. This has led to a significant rise in nonlinear components within the power grid, accompanied by an increase in harmonic components [11], [12]. Consequently, the quality of electric energy decreases, resulting in increased power grid losses. Such conditions can severely shorten the lifespan of electrical equipment and disrupt the normal functioning of communication systems. Therefore, effective measures must be taken to control the harmonics in the power system. To achieve better harmonic control, accurate detection of the increased harmonic information in the power system is essential. In power grid with asymmetrical or harmonic voltages, the PLL introduces harmonic components, such as the second frequency, into the dq component, leading to errors in amplitude and phase detection. The most commonly utilised phase-locking technique in ideal three-phase grid-connected systems is the synchronous reference frame PLL (SRF-PLL). To enhance the performance of SRF-PLL in non-ideal power grids, several studies have focused on improving its capabilities [13], [14]. References [15], [16] utilise a delay signal cancellation (DSC) algorithm to suppress harmonic interference and demonstrate good filtering performance. However, the control loop introduces inherent delay through the delay link, which can impact the dynamic

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behaviour of the PLL. Consequently, it fails to meet the requirement of tracking the fundamental frequency of the power grid within 2 to 3 power frequency cycles under three-phase imbalance conditions. In Reference [17], an adaptive Clark transform is utilised to achieve precise phase locking, even when there are imbalances in the amplitude and phase of the three-phase voltage. It utilises a band-pass filter for filtering purposes and provides a phase error correction algorithm. However, this approach suffers from complex structure and heavy computational burden. Although References [18], [19] propose a simpler phase method compared to previous approaches, they do not fundamentally analyse the internal relationship between phase imbalance and phase locking errors. Reference [20] presents a design scheme for a cascaded proportional-integral-differential (PID) controller based on the approximate model of a moving average filter (MAF). The PID parameter tuning in this scheme is performed using the MAF approximate model, neglecting notch characteristics. Compared to traditional MAF-PLL, this approach exhibits significantly improved response speed but reduced steady-state immunity. Moreover, as the amplitude of grid frequency offset exceeds the rated power frequency, the phase angle tracking error increases noticeably. In reference [21], a novel approach is introduced where the MAF is positioned at the front stage of the control loop instead of inside the PLL control loop. The enhanced pre-filtering approach greatly improves the adjusting time of the MAF-PLL. However, implementing this approach can be complex. In Reference [22], a combined loop filter consisting of a differential filter and a PID controller is employed. This leads to the development of a PID multi-complex coefficient filter PLL (MCCF-PLL). The MCCF-PLL demonstrates improved dynamic response compared to previous methods. However, it still encounters accuracy issues when confronted with high harmonic conditions.

To eliminate the above drawbacks, this paper introduces a dual second-order all-pass filter (DSOAPF) as a solution. The proposed approach involves utilising a combined filter consisting of a DSOAPF and a comb filter (CF) within the QT-PLL structure. This enables the PLL to accurately detect synchronous voltage signals even in scenarios where the three-phase voltage has negative sequence components, harmonic components, and DC components simultaneously. The proposed PLL demonstrates accurate tracking of voltage, phase, and frequency in the three-phase voltage. It operates stably even in the presence of unbalanced power grid voltages and high-order harmonics.

The main contributions of this paper are as follows:

1. A DSOAPF filter is designed to be applied in three-phase grid environment, which can be used in PLL to filter out the fundamental negative sequence voltage component and extract the fundamental positive sequence voltage component.
2. A combined filter based on DSOAPF and CF is proposed, which can help the PLL to accurately obtain the phase information of the grid voltage, and at the same time, filter out the interference of harmonic voltages in the PLL.
3. The proposed DSOAPF-CF-PLL has better dynamic adjustment ability, and its superior dynamic performance makes it suitable for grid synchronisation applications of grid connected converters.

The paper is structured as follows: Section 2 introduces the structure and working principle of the DSOAPF which is proposed in this study. In Section 3, a combined filter based on DSOAPF and CF is presented. The novel PLL is then designed based on this combined filter. The parameters of the novel PLL is analysed. Section 4 verifies the performance of the proposed PLL through comparative simulation experiments and compares the proposed PLL with other high-performance PLLs to further validate its effectiveness. Section 5 concludes the paper, summarising the findings and contributions of this study.

2. Implementation of the Dual Second-Order All-Pass Filter

2.1 Second-Order All-Pass Filter

To address the impact of fundamental negative sequence component (FNSC) in asymmetric single-phase power grids and accurately obtain power grid frequency information, Reference [23] introduces a frequency-locked loop based on a second-order all-pass filter (SOAPF) structure as depicted in Fig. 1.

In Fig. 1, the input signals are denoted as u and the output signals are represented by v_a and v_b. The signal $\widehat{\omega}$ is used for frequency estimation, while k represents the gain value. The input-output relationship expression of the all-pass filter (APF) structure in Fig. 1 is:

$$G_{\mathrm{APF}}(s) = \frac{\widehat{\omega} - s}{s + \widehat{\omega}} \tag{1}$$

The transfer function of SOAPF can be obtained by combining APF structure into second-order system as follows:

$$G_a(s) = \frac{v_a(s)}{u(s)} = \frac{k\widehat{\omega}(\widehat{\omega} + s)}{s^2 + k\widehat{\omega}s + (1+k)\widehat{\omega}^2} \tag{2}$$

$$G_b(s) = \frac{v_b(s)}{u(s)} = \frac{k\widehat{\omega}(\widehat{\omega} - s)}{s^2 + k\widehat{\omega}s + (1+k)\widehat{\omega}^2} \tag{3}$$

According to Reference [23], the desirable value for k is 1.414, which corresponds to the bode diagrams of $G_a(s)$ and $G_b(s)$ shown in Fig. 2. From Fig. 2 and (2) and (3), it can be observed that the amplitude curves of $G_a(s)$ and $G_b(s)$ coincide. Therefore, they can be considered as second-order band pass filters. In a single-phase system, their combination effectively filters out the FNSC.

2.2 Novel Dual Second-Order All-Pass Filter

Although the SOAPF is originally designed for single-phase systems, it needs to be applied in three-phase PLL systems too. In a three-phase grid-connected system,

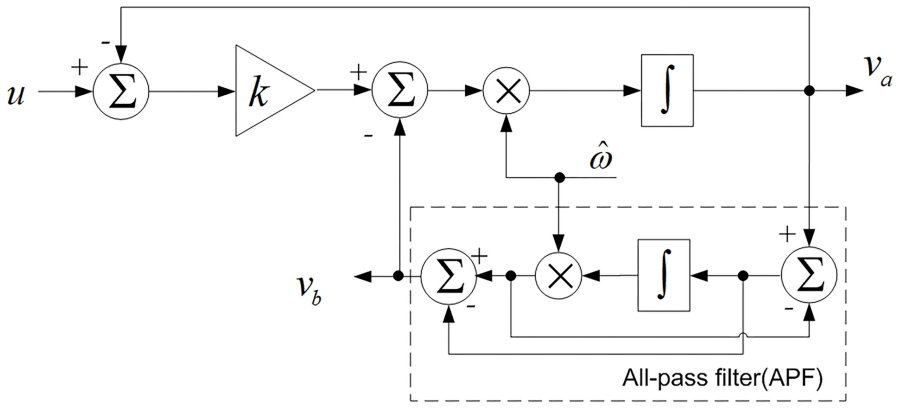

Figure 1. Structure diagram of SOAPF.

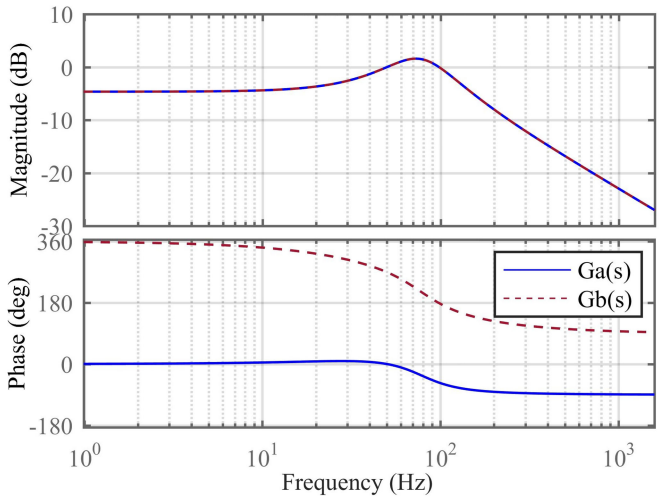

Figure 2. Bode diagram of $G_a(s)$ and $G_b(s)$.

PLL typically utilises two filters combined with a positive sequence calculator (PSC) to extract the fundamental positive sequence component (FPSC) of the grid voltage. In this paper, the proposed DSOAPF consists of two SOAPF structures and a PSC. The DSOAPF filter not only extracts the FPSC but also eliminates the FNSC.

The proposed DSOAPF's structure is shown in Fig. 3, it can be represented by the following mathematical relationship:

$$\begin{bmatrix} \widehat{v}^{+}_{\alpha,1} \\ \widehat{v}^{+}_{\beta,1} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} G_a(s) & -G_b(s) \\ G_b(s) & G_a(s) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{4}$$

Where v_α and v_β represent voltage signals in the $\alpha\beta$ coordinate system obtained by transforming the three-phase voltage through an abc-$\alpha\beta$ coordinate transformation. After undergoing DSOAPF filtering, the resulting signals $\widehat{v}'_\alpha$, $\widehat{v}''_\alpha$, $\widehat{v}'_\beta$, and $\widehat{v}''_\beta$, when passed through the PSC module, output only FPSC signal as signals $\widehat{v}^{+}_\alpha$ and $\widehat{v}^{+}_\beta$. Utilising the complex variable filter approach [24], the DSOAPF filter in the $\alpha\beta$ coordinate system can be

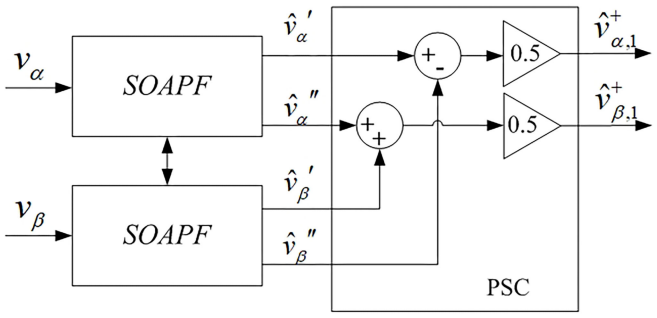

Figure 3. Block diagram of DSOAPF.

expressed as follow:

$$\begin{aligned} \mathrm{DSOAPF}(s) &= \frac{1}{2}(R_{\mathrm{DSOAPF}}(s) + jQ_{\mathrm{DSOAPF}}(s)) \\ &= \frac{1}{2}\frac{k\widehat{\omega}(\widehat{\omega}+s) + jk\widehat{\omega}(\widehat{\omega}-s)}{s^2 + k\widehat{\omega}s + (1+k)\widehat{\omega}^2} \end{aligned} \tag{5}$$

Among them

$$R_{\mathrm{DSOAPF}}(s) = G_a(s) = \frac{k\widehat{\omega}(\widehat{\omega}+s)}{s^2 + k\widehat{\omega}s + (1+k)\widehat{\omega}^2} \tag{6}$$

$$Q_{\mathrm{DSOAPF}}(s) = G_b(s) = \frac{k\widehat{\omega}(\widehat{\omega}-s)}{s^2 + k\widehat{\omega}s + (1+k)\widehat{\omega}^2} \tag{7}$$

When k is 1.414, Fig. 4 displays the bode plot of DSOAPF(s).

Observing Fig. 4, it is evident that in the $\alpha\beta$ coordinate system, the amplification value of DSOAPF(s) at -50 Hz is $-\infty$. This indicates that the FNSC in the grid voltage can be effectively suppressed by DSOAPF. At 50 Hz, the amplification factor of DSOAPF(s) is 0, and its corresponding phase allows for accurate and complete extraction of the FPSC. Consequently, this DSOAPF(s) successfully achieves the task of fully extracting the FPSC.

When it is necessary to use DSOAPF in the inner loop of a PLL, it needs to be converted into the dq coordinate system to achieve dqDSOAPF. The transfer function for implementing dqDSOAPF can be obtained by replacing s

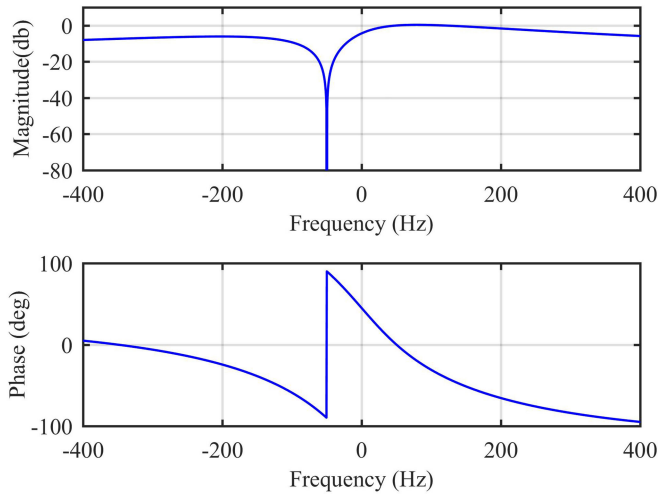

Figure 4. Bode plot of DSOAPF (s).

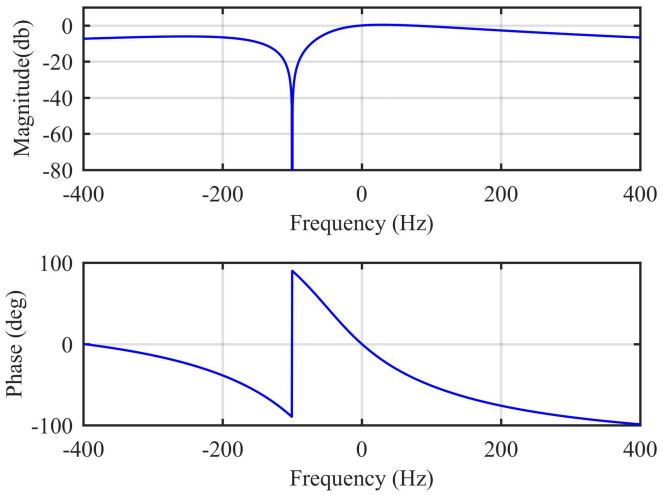

Figure 5. Bode diagram of dqDSOAPF(s).

in DSOAPF(s) with $s + j\widehat{\omega}$ as follow:

$$\begin{aligned} \text{dqDSOAPF}(s) &= \text{DSOAPF}(s + j\widehat{\omega}) \\ &= \frac{1}{2}\frac{k\widehat{\omega}(\widehat{\omega} + s + j\widehat{\omega}) + jk\widehat{\omega}(\widehat{\omega} - s - j\widehat{\omega})}{(s + j\widehat{\omega})^2 + k\widehat{\omega}(s + j\widehat{\omega}) + (1 + k)\widehat{\omega}^2} \end{aligned} \tag{8}$$

The bode diagram of dqDSOAPF is depicted in Fig. 5. It shows that in the dq coordinate system, the amplification factor of dqDSOAPF at -100 Hz, corresponding to the FNSC is $-\infty$. Therefore, dqDSOAPF can effectively suppress the FNSC while still being able to accurately extract both FPSC and FNSC [25].

3. The PLL Design Based DSOAPF and CF

To mitigate the impact of power grid harmonics on the phase tracking of a PLL in a distorted environment, this paper introduces the CF. The CF filter is utilised with the proposed DSOAPF to create a combined filter. This combined filter is then incorporated into a quasi-type-1 PLL (QT1-PLL) to design a novel PLL which is called DSOAPF-CF-PLL [26]. Figure 6 depicts the structure of DSOAPF-CF-PLL.

In Fig. 6, the CF transfer function is

$$\text{CF}(s) = \left(\frac{1 - e^{-T_\omega s}}{T_\omega s}\right)^n \tag{9}$$

Where $T_\omega = T/6$, T is 20 ms, n takes 1 [27], [28].

Moreover, the transfer function of the combined filter is:

$$\begin{aligned} H(s) &= \text{dqDSOAPF}(s)CF(s) \\ &= 1/2\frac{k\widehat{\omega}(\widehat{\omega} + s + j\widehat{\omega}) + jk\widehat{\omega}(\widehat{\omega} - s - j\widehat{\omega})}{(s + j\widehat{\omega})^2 + k\widehat{\omega}(s + j\widehat{\omega}) + (1 + k)\widehat{\omega}^2}\left(\frac{1 - e^{-T_\omega s}}{T_\omega s}\right)^n \end{aligned} \tag{10}$$

According to (10), Fig. 7 represents the bode plot of the combined filter. The diagram demonstrates that the combined filter H(s) effectively filters out the FNSC and major harmonic voltages, such as the -5th, $+7$th, -11th, and $+13$th in the three-phase power grid voltage. Additionally, it directly extracts the FPSC information from the grid voltage. This indicates its suitability for utilisation within PLL even in the presence of distortion conditions.

To simplify the parameter selection process and determine the value of kp, this section establishes simulation models of the DSOAPF-CF-PLL using MATLAB/Simulink. Additionally, to ensure a faster response speed and desirable convergence characteristics when the grid voltage changes, the phase jump tests are designed for DSOAPF-CF-PLL with different values of k_p. Figure 8 illustrates the estimated frequency curves obtained from these phase jump tests with varying k_p values. From the plot, it can be observed that when the k_p value for the DSOAPF-CF-PLL is chosen as 80, the convergence of the curves is optimal, and the response speed is faster compared to other values of k_p. These selected k_p values ensure improved performance and meet the desired requirements of the designed system.

The structure of the DSOAPF-CF-PLL is illustrated in Fig. 6. This structure is mathematically modeled using a similar approach to QT1-PLL. The small-signal model and its simplified model are shown in Figs. 9 and 10.

Based on Fig. 10, the mathematical expression for the open-loop transfer function of the PLL mathematical model can be obtained as follows:

$$G_{\text{ol}}(s) = \left(\frac{\text{dqDSOAPF}(s)CF(s)}{1 - \text{dqDSOAPF}(s)CF(s)}\right)\left(\frac{s + k_p}{s}\right) \tag{11}$$

After obtaining the kp values for the DSOAPF-CF-PLL, this paper employs the Nyquist stability criterion to assess the stability of the system. Figure 11 illustrates the Nyquist curve for DSOAPF-CF-PLL according to (11).

From Fig. 11, it is evident that the open-loop transfer function of the DSOAPF-CF-PLL system does not encircle (-1, j0). This observation serves as evidence that the closed-loop system corresponding to the DSOAPF-CF-PL is stable.

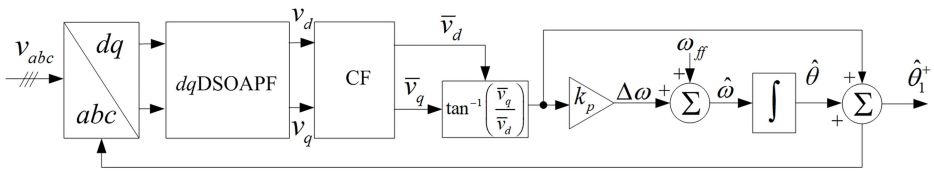

Figure 6. Structure of DSOAPF-CF-PLL.

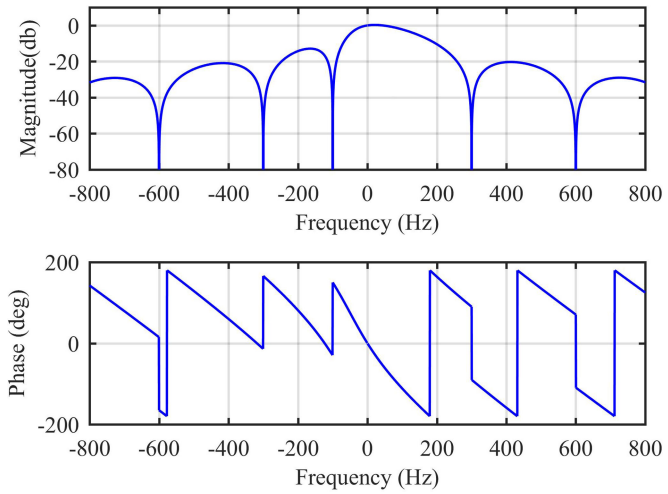

Figure 7. Bode plot of the combined filter.

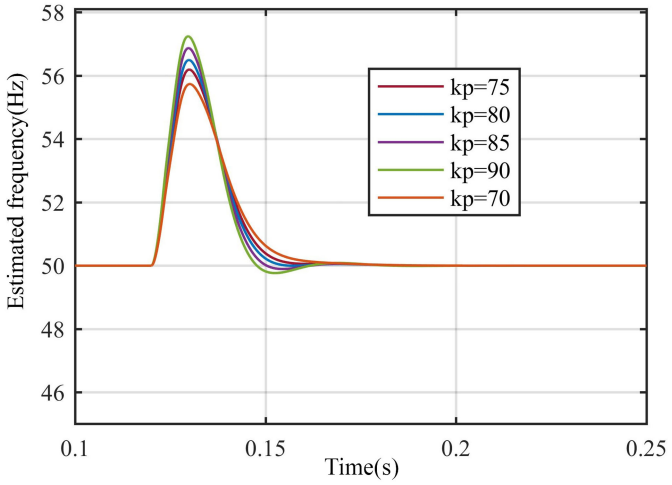

Figure 8. Diagram of different values of k_p.

4. Simulation Experiments

To test the behaviour of the DSOAPF-CF-PLL, simulation experiments are conducted using MATLAB/Simulink software under four types of faults: frequency abrupt change, harmonic injection, rapid voltage sag, and frequency ramp change. During the simulation, the power grid frequency is set to 50 Hz, the amplitude of the three-phase voltage is normalised to 1 p.u. (per unit), and the sampling frequency is set at 10 kHz.

To demonstrate the superiority of the PLL proposed in this paper, two conventional PLLs (MCCF-PLL [29], [30] and DMAF-PLL [31]) are included for comparison. The proportional parameter k_p value of the proposed PLL in this paper is set to 80, the proportional coefficient k_{p-MCCF} value of MCCF-PLL is 141.2, the integral coefficient k_{i-MCCF} value of MCCF-PLL is 9,928, the proportional coefficient k_{p-DMAF} value of DMAF -PLL is 250, the integral coefficient k_{i-MCCF} value of DMAF-PLL is 26,041.

Figure 12 is the waveform diagram when the frequency abrupt change of + 6 Hz occurs, where Fig. 12(a) is the voltage operation diagram and Fig. 12(b) and 12(c) are frequency and phase estimation diagrams, respectively. As can be seen from Fig. 12, after a brief adjusting process, the phase errors of these PLLs can fallback to 0, and accurate frequency tracking can be achieved. However, the transient process of DSOAPF-CF-PLL proposed in this paper is faster, and it only takes about 25 ms to converge to zero, while the transient convergence time of DMAF-PLL is the second, and the transient convergence time of MCCF-PLL is the slowest. In addition, compared with DMAF-PLL and MCCF-PLL, the frequency estimation overshoot of DSOAPF-CF-PLL proposed in this paper is the smallest, and its curve is smoother from its waveform, while the frequency estimation overshoot of DMAF-PLL and MCCF-PLL is larger.

Figure 13 depicts a waveform diagram of the grid voltage with an added harmonic voltage and a phase jump of 35°. Figure 10(a) is the voltage operation diagram, Fig. 13(b) and Fig. 13(c) are the frequency and phase estimation diagrams, respectively. According to Fig. 13, it is evident that the DSOAPF-CF-PLL effectively eliminates the major harmonics present in the power grid, resulting in a relatively smooth curve. Although DMAF exhibits some filtering function, the influence of harmonics on its phase-locked function is still noticeable from its curve, and its frequency estimation curve exhibits slight ripple, which can lead to significant overshoot. Furthermore, as shown in Fig. 13(c), the transient convergence length of the DSOAPF-CF-PLL is slightly shorter compared to the other two PLLs, while the state convergence time of the other two PLLs is slightly longer.

Figure 14 illustrates a waveform diagram depicting a 50% drop in grid voltage in two phases. Fig. 14(a) is the voltage operation diagram, Fig. 14(b) and 14(c) represent the frequency and phase estimation diagrams, respectively. From Fig. 14(b), it is apparent that the proposed DSOAPF-CF-PLL experiences a quick transient convergence process after the occurrence of the grid voltage sag, exhibiting the shortest dynamic time. Although the transient convergence process of DMAF-PLL and MCCF-PLL takes longer and their curves display larger oscillation amplitudes, their performance is inferior to that of the

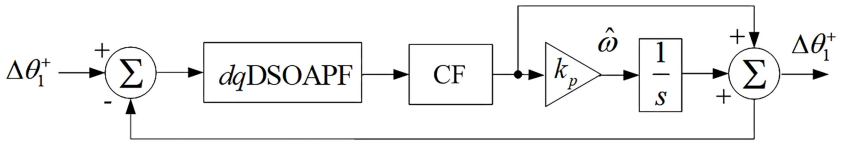

Figure 9. Small-signal model of the DSOAPF-CF-PLL.

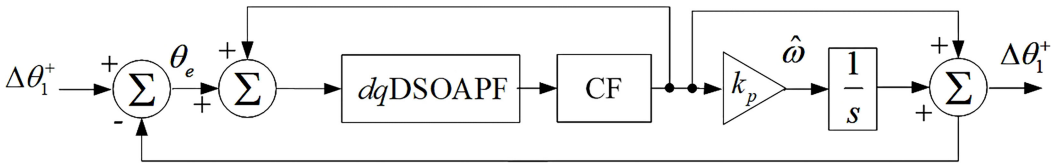

Figure 10. Simplified model of the DSOAPF-CF-PLL.

Table 1
Simulation Experimental Results of the Three PLLs Used in this Paper

		DSOAPF-CF-PLL	MCCF-PLL	DMAF-PLL
Sudden change of grid voltage frequency	Settling time	25 ms	51 ms	29 ms
	Estimated phase error overshoot	9.8°	14.2°	7.8°
	Estimated frequency overshoot	0 Hz	2.5 Hz	1.7 Hz
Harmonic distortion with Sudden change of grid voltage phase	Settling time	31 ms	36 ms	32 ms
	Estimated phase error overshoot	11.1°	17.2°	9.3°
	Estimated frequency overshoot	6.1 Hz	11.8 Hz	28.7 Hz
50% voltage drop	Settling time	39 ms	62 ms	55 ms
Slow change of grid voltage frequency	Phase-error	1.4°	2.8°	1.7°

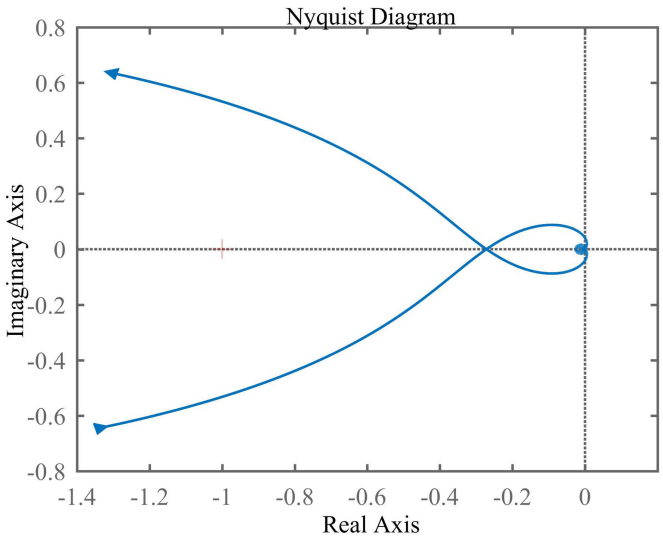

Figure 11. Nyquist curve of the DSOAPF-CF-PLL open loop transfer function.

DSOAPF-CF-PLL proposed in this paper. Moreover, as seen in Fig. 14(c), the transient convergence length of the DSOAPF-CF-PLL is slightly shorter, while the state convergence time of the other two PLLs is slightly longer. On the other hand, the filtering function of MCCF-PLL is mainly achieved through the CCF module, which does not provide thorough filtering. The frequency estimation curve of MCCF-PLL displays uniform small amplitude ripples, affecting accuracy.

Figure 15 illustrates the experiential waveforms when frequency change slowly in power grid. The frequency shift occurs at 0.12 s, and after 0.08 s, the grid frequency gradually increases from 50 Hz to 56 Hz. Figure 15(a) is the voltage operation diagram, Figs. 15(b) and 15(c) represent the frequency and phase estimation diagrams, respectively. Observing Fig. 15(b), it is evident that the DSOAPF-CF-PLL proposed in this paper quickly returns to its normal state following the frequency change. In contrast, both DMAF-PLL and MCCF-PLL exhibit slower recovery times and some degree of overshoot, indicating inferior dynamic recovery performance compared to DSOAPF-CF-PLL. Additionally, examining Fig. 12(b) demonstrates that the proposed DSOAPF-CF-PLL in this paper achieves a phase tracking error of at most 1.4°. DMAF-PLL follows with an error of 1.7°, while the worst error for MCCF-PLL is 2.8°. Thus, among the three PLLs, the DSOAPF-CF-PLL offers the highest phase-locked accuracy.

Table 1 presents a comparative statistical analysis of the simulation experimental results obtained from the three PLLs in this paper. Based on the simulation

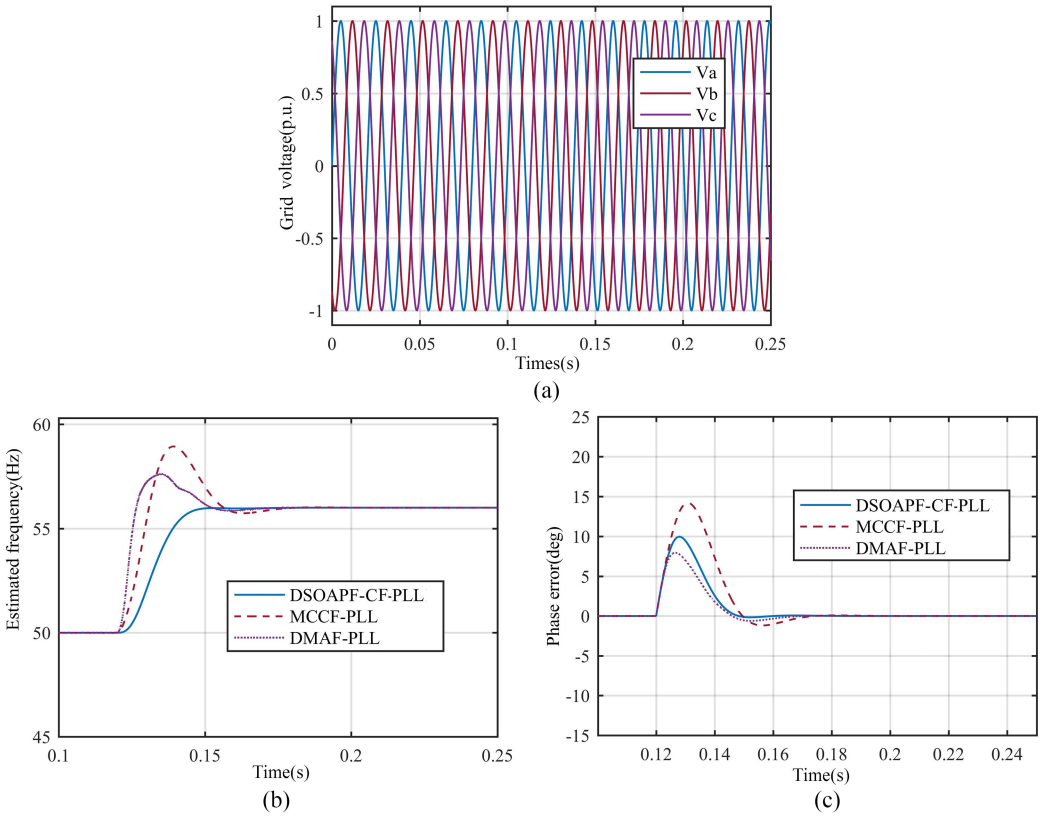

Figure 12. Experiential waveforms when frequency change occurs in power grid.

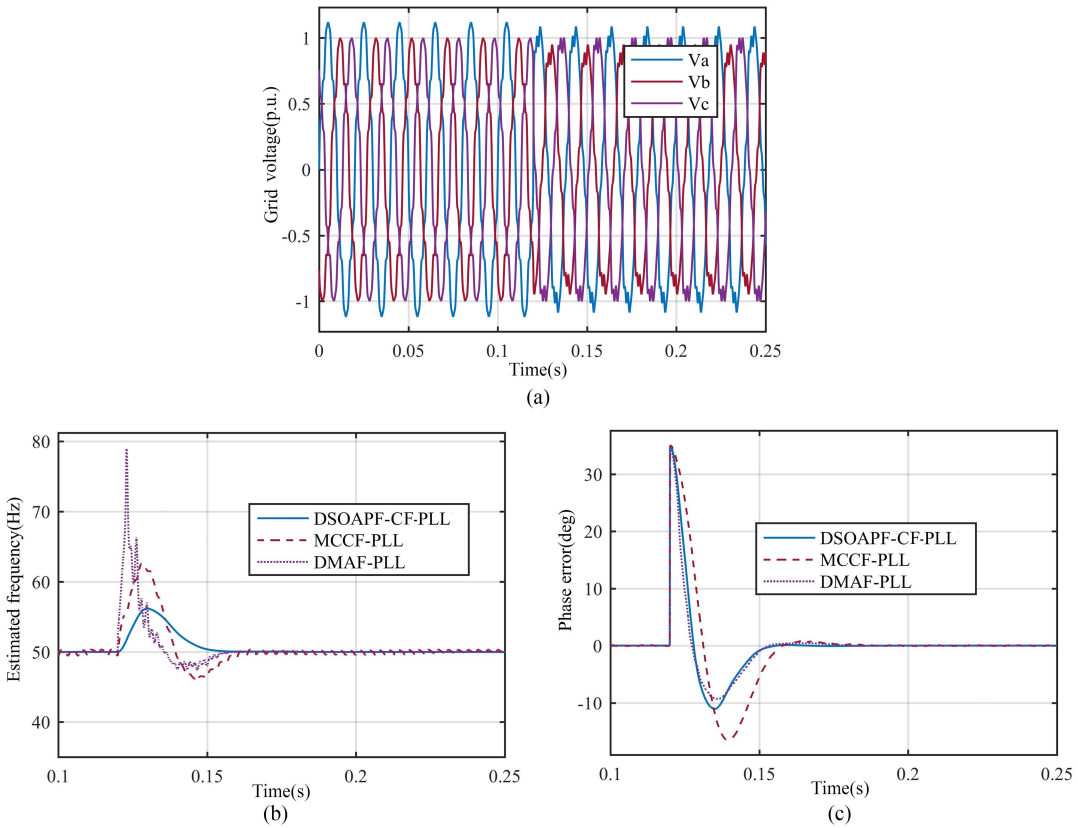

Figure 13. Experiential waveforms when grid voltages are added into harmonic voltages and phase jumps.

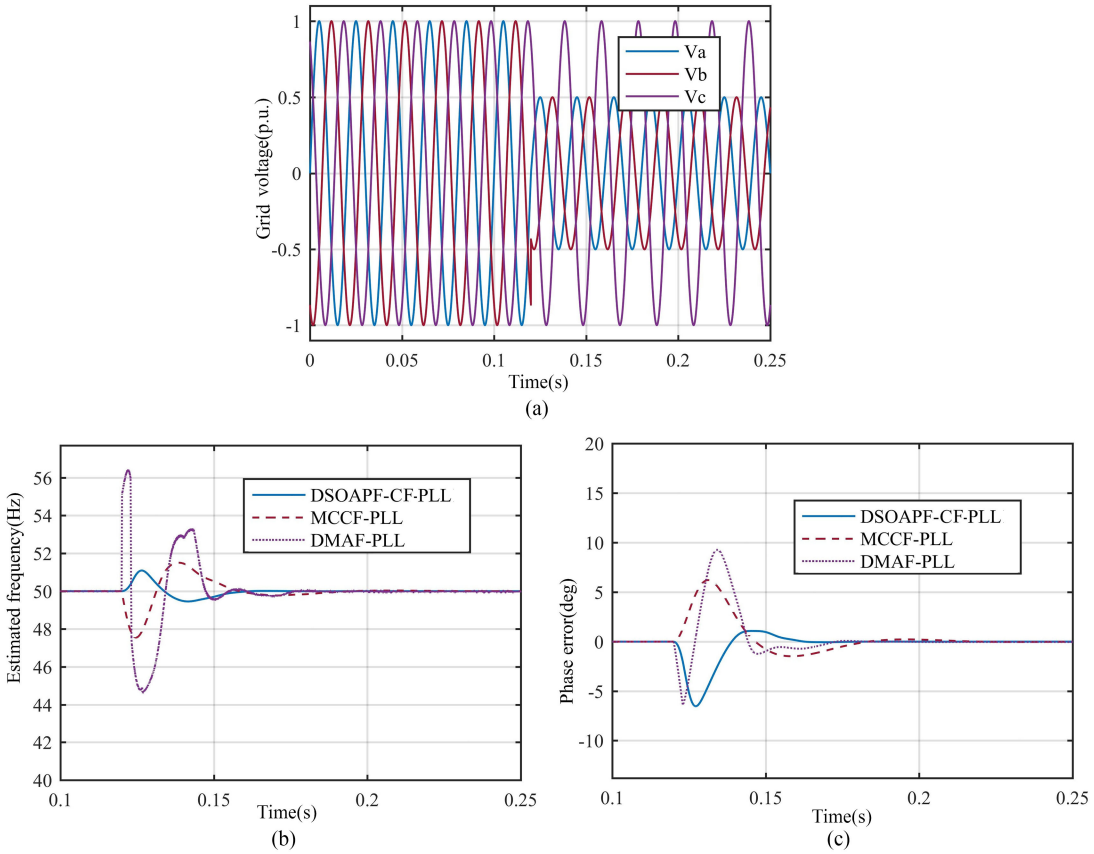

Figure 14. Experiential waveform depicting a 50% drop in grid voltage in two phases.

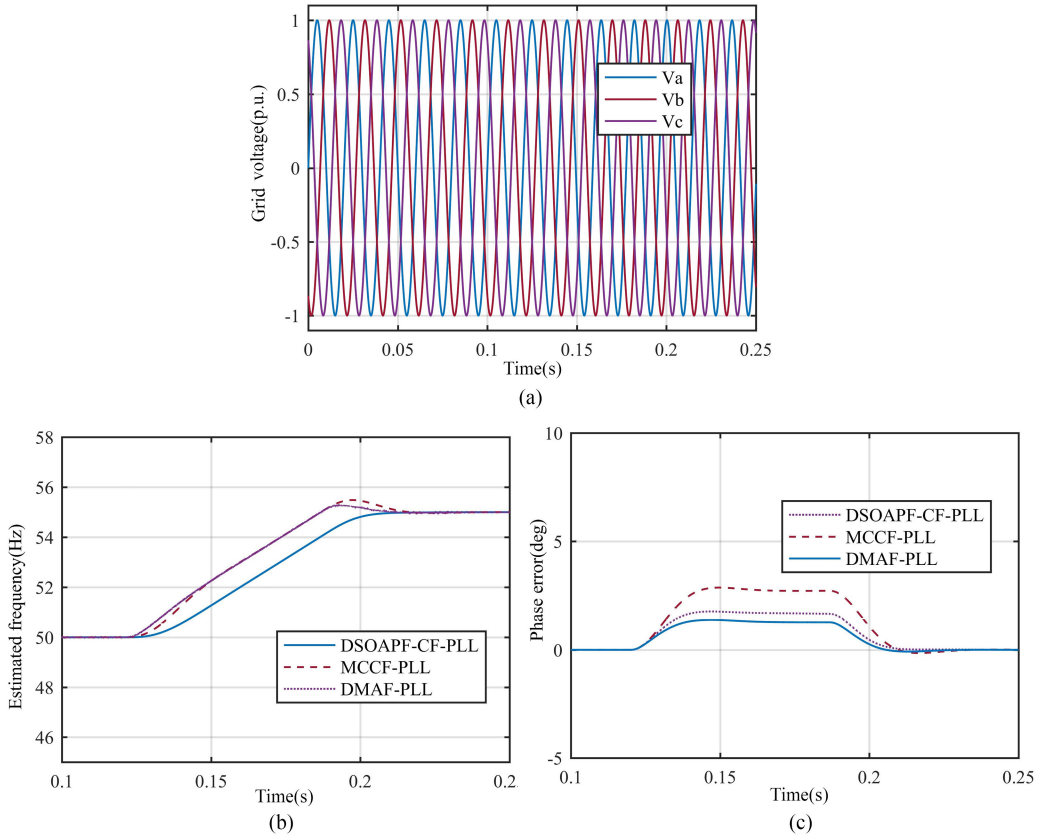

Figure 15. Experiential waveforms when frequency change slowly in power grid.

results presented above, it can be concluded that the DSOAPF-CF-PLL exhibits the fastest convergence time among the power grid applications. In comparison with DMAF-PLL and MCCF-PLL, the proposed DSOAPF-CF-PLL in this paper demonstrates faster dynamic response characteristics and smaller overshoot. Therefore, the PLL method introduced in this paper is considered more suitable for practical grid-connected applications.

5. Conclusion

To address the issues of poor phase-locked precision resulting from unbalanced voltage and a high amount of harmonics during the grid-connected process, this article designs a DSOAPF filter based on SOAPF. Additionally, a combined filter is constructed by combining DSOAPF with CF, and a novel PLL based on this combined approach is introduced. The simulation results demonstrate that the DSOAPF-CF-PLL exhibits superior dynamic performance compared to the other two traditional two methods, it can improve dynamic characteristics by over 10% compared to the other two methods. In addition, the method has superior filtering characteristics. As a result, it is deemed more suitable for grid-connected new energy applications than conventional approaches.

Acknowledgement

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