COMPACT, MULTI-CHANNEL, ELECTRONIC INTERFACE FOR PNS RECORDING AND STIMULATION

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ABSTRACT
A multi-channel system for neural signal recording/stimulation is presented. The system is split on two devices: an implantable High Voltage (HV) CMOS integrated circuit (IC) hosting a sigma delta modulator, together with a low noise preamplifier/prefilter and a digital platform for sigma delta decimation/control implemented on a FPGA. This innovative approach guarantees a robust communication link while minimizing the blocks to be implanted, saving power and area. The recording unit exhibits an $IRN = 2.12\mu V_{rms}$ in $800Hz - 8kHz$ bandwidth, a programmable gain in the range $45.4dB - 58dB$ and a 14-bit A/D conversion. The IC hosts also a current-mode stimulator able to deliver currents in the range of hundreds of microampere to electrodes with impedances up to $100k\Omega$.

KEY WORDS
Neural recording, PNS stimulation, Biomedical interfaces, Sigma delta converters, Low noise neural amplifier.

1 Introduction

In last decades many advances towards the development of implantable neural interfaces have been achieved. On one hand, the introduction of new biocompatible materials has made chronic implant of electrodes feasible [1]. On the other hand the increasing capability of developing small-size integrated circuits with high performances and low power consumption has made possible the design of new devices whose dimensions are compatible with a permanent implant. Many diseases can benefit from the use of this kind of devices. In the field of neuroprosthetics, for instance, neural interfaces offer the possibility to realize a bidirectional communication between the Peripheral Nervous System (PNS) and a robotic limb thus paving the way for a true embodiment of the prosthesis. For such reason, an integrated circuit that implements a recording-stimulation neural interface aimed to control a prosthetic hand by means of signals extracted with intra-fascicular electrodes implanted in the PNS is presented. Bidirectional interfaces including both the recording and the stimulation modules have been presented in [2, 3, 4]. Due to the nature of the neural signals, the front-end stage of a recording unit is composed of 3 main parts: a low noise amplifier, a Band Pass Filter (BPF) and an Analog to Digital Converter (ADC). Since the typical neural amplitudes are in the range $20\mu V - 100\mu V$, the first stage in the chain flow must be a low noise amplifier [5, 6, 7] to boost the signal before any other processing avoiding signal corruption. The filtering operation is particularly important, the nerves, in fact, are surrounded by the muscles, whose electrical signals (EMG), are characterized by large amplitudes (in the millivolt range) and by frequencies very closed to those of neural signals. Such interferences may mask the neural signal or saturate the amplifier thus must be properly filtered [7]. Since the typical noise floor level due to electrodes noise and spontaneous neural activity is around $10\mu V$ in a $10kHz$ bandwidth [8], A/D conversion is usually implemented with only 8-10 bit resolution [5] thus exploiting a successive-approximation (SA) architecture [8, 5, 6]. Nevertheless, recent research on decoding of patient movement intention from peripheral neural signals has shown that higher resolutions may be useful to properly feed the algorithms especially when intra-fascicular electrodes are used [9]. For this reason we propose an alternative approach based on oversampling converters. The system is composed by an on-chip analog front-end which includes a low-noise preamplifier/prefilter and a sigma delta modulator and by a digital platform, realized off-chip on a FPGA. The main aim is to shift the complexity of A/D conversion and selective filtering in the digital domain, keeping the implantable analog module as simple as possible. Such approach implies a number of advantages in terms of power and area reduction, exploiting the integration capabilities of digital circuits that allow to easily design high order digital filters without having a large area occupancy. The choice to implement an off-chip digital part, does not affect in any way the system performances, since the modulator output is already converted in a 1-bit digital signal, therefore a robust link between the analog and the digital part is guaranteed. The use of a third-order modulator and an OSR=125 allowed to reach a relatively large resolution (14-bit). A similar approach was investigated in [10], but in that case a first order sigma delta converter was designed, obtaining an 8-bit resolution with a 40 oversampling ratio over a $6.25kHz$ frequency. For what concerns the stimulation unit, the stimuli are generated through

DOI: 10.2316/J.2014.216.818-0037

a current-output Digital-to-Analog Converter (DAC) in order to make parameters as frequency, duration and intensity programmable [11]. The stimulation shapes are bi-phasic to avoid charge accumulation in the tissues and their consequent damage [12]. Because of the high value and the high variability of the electrode-tissue impedance, a stimulator working at high voltages, able to deliver the programmed current even with high impedances, is needed. The high voltage can be supplied to the output stages by a voltage booster, the most common circuit used for this purpose is based on a Dickson charge pump [13]. In this work, a voltage booster with a 4-clocks charge pump in a triple-well CMOS process [14] was used to deliver currents in the order of hundreds of microampere even with impedances up to $100k\Omega$.

2 System Architecture

The architecture of the proposed system is presented in Fig.1. The blocks highlight the two different units that perform the bidirectional communication between the PNS and the machine: the recording module acquires the signals coming from the implanted electrodes and transmits them to the artificial machine, while the stimulation module receives the stimulation parameters and generates the desired stimulation currents to be injected into the nerves through the electrodes. Both units include an analog part (hosted on the chip) and a digital part (hosted on a FPGA).

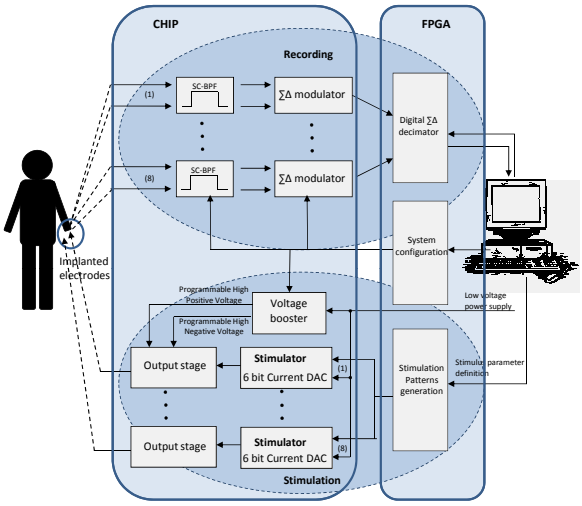


Figure 1. Block diagram of the neural recording and stimulation system.

The system has been implemented to deal with 8 channels in parallel; nevertheless it can also be used with 16 channel electrodes thanks to an input switch network that allows to select every possible combination of 8 channels among the 16 input pins. Concerning the recording module, the analog part is comprehensive of a prefiltering block and of the sigma delta modulator. The sigma delta decimator is shared among all channels and has been implemented in a FPGA Xilinx Spartan-3E 1600. The main blocks of the stimulator are the 6-bit current-output digital-to-analog converters (DAC) that generate the current waveforms; these blocks work in a low power supply domain while a high voltage supply output stage delivers the programmed current even in case of high impedance. The high voltage is supplied to the output stages by the voltage booster. The IC was designed in a $0.35\mu m$ HV CMOS process from AMS (Austriamicrosystems) with double-poly capacitors and 4 metal layers. The design kit includes both low voltage and high voltage transistors able to support up to 50V.

3 Recording Unit

The recording module has been designed using low voltage transistors with a 3.3V voltage supply. A detailed block diagram of the recording module is depicted in Figure 2. The fully differential signal path allows the common mode noise reduction and doubles the output dynamic range. The BPF, implemented as a first order High Pass Filter (HPF) cascaded with a first order Low Pass Filter (LPF), operates in the $800Hz - 8kHz$ frequency range and provides a gain that can be set between $44.5dB$ and $58dB$ [15].

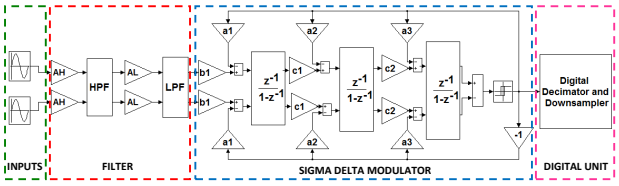


Figure 2. Recording module. The sigma delta coefficient values are: $a_1 = b_1 = 0.05$, $a_2 = 0.3$, $a_3 = 0.8$ and$c_1 = c_2 = 1$.

A single loop third order modulator, was used for the analog part of the A/D converter. The coefficients of Figure 2 were chosen using the Schreier Toolbox [16] with an 18-bit target resolution and an oversampling ratio OSR = 125. Considering a signal band of $8kHz$, the sampling frequency is $f_s = 2MHz$. The sigma delta decimator has been implemented in a FPGA, its input is the 1-bit stream generated by the modulator. This signal includes different noise components: at low frequencies, the EMG interferences, and, at high frequencies, the quantization noise shaped by the modulator. The decimator is aimed to filter the input signal with a high order digital BPF and to downsample the signal to bring back the sampling frequency at the Nyquist rate. The BPF was implemented as a 16^{th} order IIR Butterworth fixed-point filter whose main parameters are summarized in Table 1. The digital IIR filter has been shared among all the 8 channels. A solution based on Time Division Multiplexing (TDM) has been adopted in order to re-use the same hardware [17]. For this purpose, a sampling frequency of $16MHz$ (that is eight times the value

necessary for each channel) has been used.

Table 1. Digital filter parameters

Response Type	Band-Pass Filter
Design Method	IIR Butterworth
Filter Arithmetic	Fixed-Point
Passband	0.8 - 8 KHz
Input Sampling Frequency	2 MHz
Order	16
Coefficient Word Length	32 bit
Input Word Length	32 bit
Input Fraction Length	22 bit
Output Word Length	32 bit
Rounding Mode	Floor
Overflow Mode	Wrap

4 Stimulation Unit

The stimulation unit is able to deliver current pulses whose shape and parameters are represented in Figure 3 and Table 2.

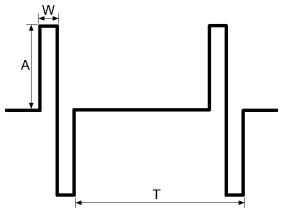


Figure 3. figure

Biphasic neural stimulus waveform.

Table 2. Typical parameters of a neural stimulation pulse.

parameter	range
Amp. (A)	$5\mu A - 300\mu A$
Width (W)	$50\mu s - 300\mu s$
Period (T)	$2.5ms - 100ms$

Several different stimulation modes are possible [18]. In this paper, a stimulator based on a single supply with anodic and cathodic active phases is adopted. As depicted in Figure 4 the stimulation is enabled by closing switch $S1$ whereas with switch $S2$ it is possible to select between anodic or cathodic phase. A switch $S3$ has also been introduced to periodically shortcut the two electrode terminals removing the residual charge accumulated at the electrode-nerve interface and avoiding, by this way, any risk of tissue damaging.
The stimulation module consists of a current DAC, an output stage and a voltage booster. As already mentioned, the

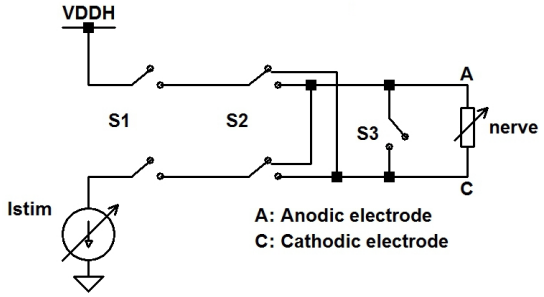


Figure 4. Single supply with anodic and cathodic active phases stimulator diagram.

stimulator is based on a low voltage 6-bit current DAC used to set the stimulation current level. The current is then converted from a low into a high voltage signal by the output stage and injected into the nerve. The high voltage supply for the output stage is generated by the voltage booster, that increases the voltage up to $20V$. The stimulation unit and, particularly, the voltage booster have been designed achieving a good compromise between size and boosting time. The voltage booster block, as depicted in Figure 5, is composed by 12 boosting cells with a final accumulation capacitor $C_{acc} = 20nF$ needed to reach $20V$ of output voltage and to deliver a load current up to $300\mu A$ for a maximum time of $300\mu s$. The booster is controlled by four clocks at $2.5MHz$ with different phases and duty-cycles.

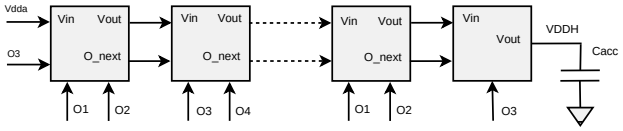


Figure 5. 12 stages voltage booster.

In order to avoid transistor damaging and to reduce the power consumption, the voltage supply generated by the booster can be programmed in a range between 3V and 19V thanks to a 3-bit DAC. The selection mechanism is shown in Figure 6. To save silicon area, the circuit has been implemented using isolated low voltage transistors; therefore a resistance voltage divider is used to scale the boosted voltage in the low voltage range between $0V$ and $3.3V$. Thanks to a comparator with hysteresis the booster is turned off when it reaches the programmed high voltage and it is turned on only after a 1V drop below its maximum value. The booster is powered up and down by switching its four clocks; this task is performed, according to the signal coming by the comparator, by the booster enable block.

5 Simulation Results

The recording part of the chip has been completed at layout level as shown in Figure 7. The results presented in this

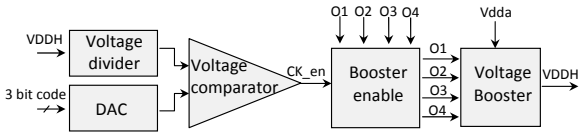


Figure 6. Boosting module's architecture.

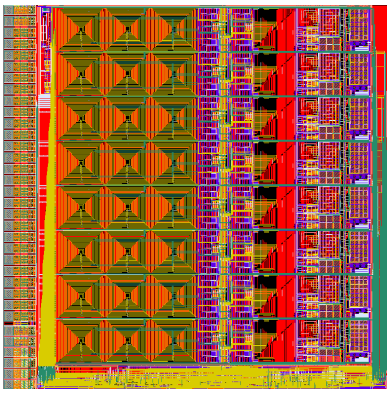


Figure 7. Recording chip layout.

section have been obtained as post-layout simulations and are, therefore, particularly accurate and reliable. Figure 8 shows the frequency response of the analog pre-filter: the black curve corresponds to the lower gain, while the grey one corresponds to the high gain configuration. In the first configuration the gain is $44.45dB$ with a $3dB$ frequency bandwidth between $790Hz$ and $7.9kHz$. The high gain configuration exhibits a $57.94dB$ gain and the 3dB bandwidth in the range $630Hz - 7.95kHz$. These values have been obtained in order to guarantee the maximum gain that avoids the amplifier saturation. The possibility to tune the gain allows to adapt the filter characteristics to the actual input and makes the system more flexible, improving the performances for a wider input dynamic range. The input referred noise for the high and the low gain configuration is respectively $3.25\mu V_{rms}$ and $2.12\mu V_{rms}$. Regarding the sigma delta modulator, its power spectral density has been calculated running a transient noise analysis from the post-layout model. Thus, the obtained results, shown in Figure 9, take into account the noise effects and should be considered highly representative of the actual converter behavior. The signal to noise ratio (SNR), obtained with an input amplitude of $0.5V$ at $3kHz$, is $85.8dB$ corresponding to 13.96 bits. Such resolution, referred to the analog prefilter, allows to detect signals lower than $1\mu V$ and is below the system noise floor calculated for the filter. In Figure 10, the relation between the SNR and the input amplitude confirms the good linearity of the converter. As expected the SNR starts to degrade for input voltages higher than $V_{ref}/2$, and, at V_{ref}, due to the signal distortion the SNR is lowered by $30dB$, while the $0dB$ is reached for less than $50\mu V$.

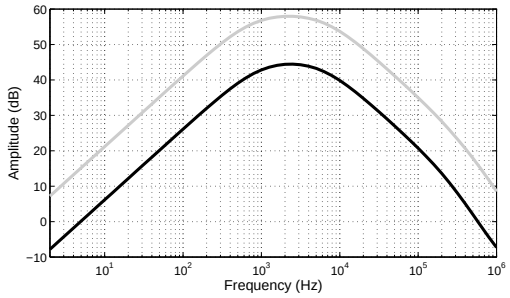


Figure 8. Bode diagram. Black curve: low gain configuration. Grey curve: high gain configuration.

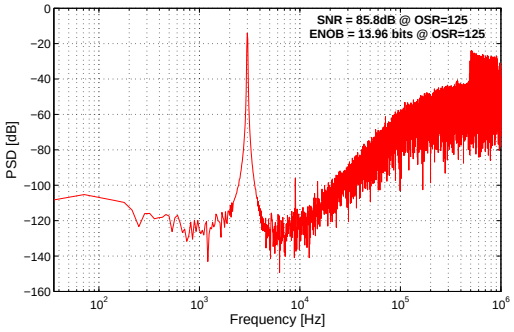


Figure 9. Sigma Delta Modulator: Power Spectral Density.

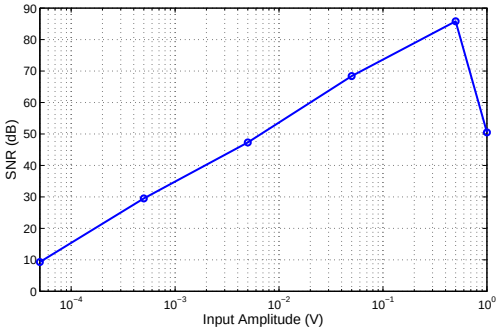
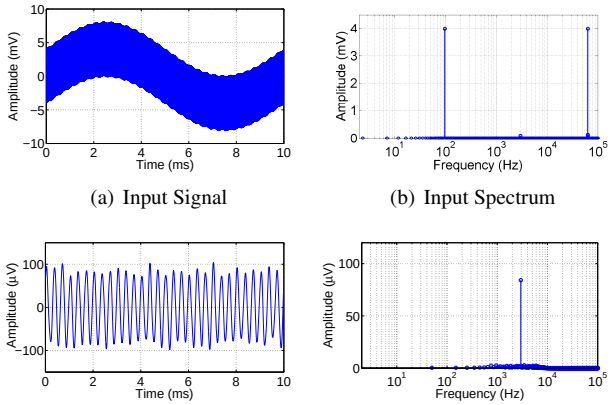


Figure 10. Sigma Delta Modulator: SNR versus Input amplitude.

The system capability to record signals with typical neural amplitudes and to filter it from huge out-of-band interferences has been tested using an input signal composed by three sine waves representing a neural component at 3kHz superimposed with two interferences at 100Hz and 64kHz. Typical neural amplitude in the tens of microvolts has been chosen for the 3kHz component, while millivolt level signals represent the interferences at low and high frequency. In Figure 11(a) and 11(b), the input signal in the time and in the frequency domain is shown. As it can be observed in

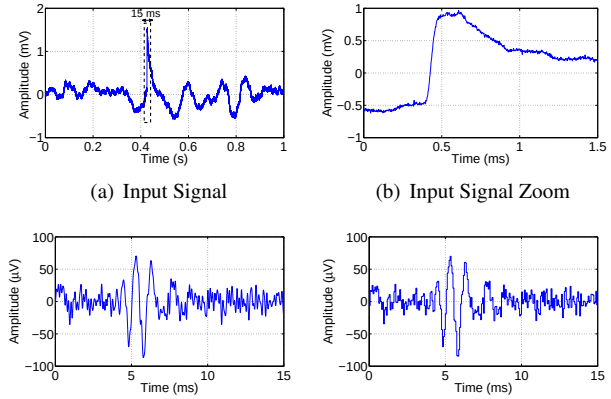
Figure 11(c) and 11(d), the output signal has been completely cleaned out from the interferences and the 3kHz component is perfectly detectable.



(a) Input Signal (b) Input Spectrum

(c) Output Signal (d) Output Spectrum

Figure 11. Recording channel response to an input composed by three sines at 100Hz, 3kHz and 64kHz.



(a) Input Signal (b) Input Signal Zoom

(c) Output Signal oversampled (d) Output Signal

Figure 12. Response to a pre-recorded neural signal.

A more realistic test has been performed using real signals pre-recorded in clinical trials with rabbits. The signal was acquired with a tfLIFE electrode implanted in the sciatic nerve of the rabbit during lateral surface buzzing on the animal foot. Figure 12(a) shows one-second of recording trace, it is characterized by low frequency interferences due to different environmental noise sources. A shorter interval of 15ms within this recording trace, has been chosen as input for the post-layout simulation. This signal is highlighted with the dotted box and zoomed in Figure 12(b). The trace has been processed by the analog pre-filter with a 780V/V gain and converted in the digital domain with the sigma delta ADC. The results are shown in Figure 12(c) and 12(d) where, respectively the oversampled signal at the digital filter output and the downsampled signal generated by the decimator, are reported. The results show how the input signal has been cleaned up and the presence of two neural spikes, which in the input signal were masked by the huge EMG interferences, is now evident.

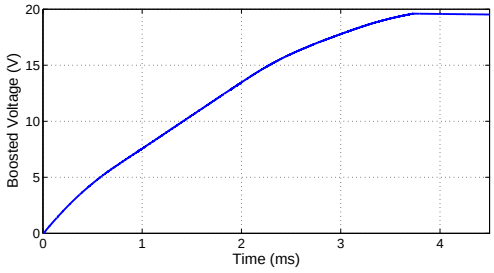


Figure 13. Voltage boosted to 19V.

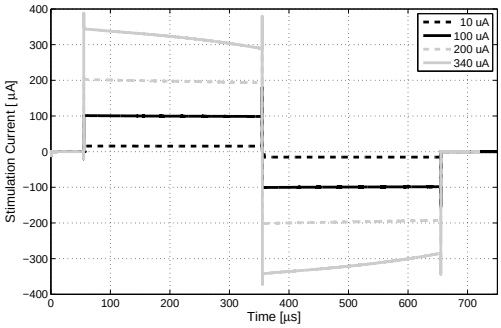


Figure 14. Stimulation current programmability.

The voltage booster has been successfully tested. As shown in Figure 13, it has been programmed to reach $19V$ and, as expected, after a boosting time of $3.7ms$, the voltage stops to rise and settles to $19V$. The currents generated by the output stage with the boosted voltage are shown in Figure 14 for different amplitude values and for a pulse width of $300\mu s$. It can be noticed that, in the highest value ($340\mu A$) case, the current drops markedly. This phenomenon occurs for currents higher than $300\mu A$ and is due to the accumulation capacitor discharging. Since the range of interest seems to be below $300\mu A$, this fact should not be considered a problem. In any case, the current depends upon the off-chip accumulation capacitor and can, therefore, be increased without changing the ASIC design.

6 Conclusion

In this paper a novel system for peripheral neural signal recording and stimulation has been presented. The device, developed on an IC for the analog part and on a FPGA for the digital part, allows to detect neural signals of few tens of

microvolts thanks to its low IRN of $2.12\mu V_{rms}$. The stimulation module can deliver bi-phasic current pulses with programmable amplitude, duration and frequency and works properly with electrode-tissue impedances up to $100k\Omega$. The designed chip has been successfully tested by means of postlayout simulations. Future developments envisage the chip integration with the electrode and its implantation inside the human body to control a robotic hand.

Acknowledgments

The authors would like to thank Silvestro Micera from the EPFL of Lausanne for neural traces providing. This work was partially funded by MIUR (Italian Ministry of Education, University and Research) through project HANDBOT (PRIN 2010/2011), by Italian Ministry of Health through project NEMESIS and by the European Commission, ICT-2013.9.6 FET Proactive: Evolving Living Technologies (EVLIT), through project NEBIAS (n.611687). L. Bisoni gratefully acknowledges Sardinia Regional Government for the financial support of his Ph.D. scholarship (P.O.R. Sardegna F.S.E. Operational Programme of the Autonomous Region of Sardinia, European Social Fund 2007-2013 - Axis IV Human Resources, Objective l.3, Line of Activity l.3.1.). C.Carboni and N.Carta gratefully acknowledge Sardinia Regional Government for the financial support to their research grant.

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